

NM-SpMM: Accelerating Matrix Multiplication Using $N:M$ Sparsity with GPGPU

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Abstract—Deep learning demonstrates effectiveness across a wide range of tasks. However, the dense and over-parameterized nature of these models results in significant resource consumption during deployment. In response to this issue, weight pruning, particularly through $N:M$ sparsity matrix multiplication, offers an efficient solution by transforming dense operations into semi-sparse ones. $N:M$ sparsity provides an option for balancing performance and model accuracy, but introduces more complex programming and optimization challenges. To address these issues, we design a systematic top-down performance analysis model for $N:M$ sparsity. Meanwhile, NM-SpMM is proposed as an efficient general $N:M$ sparsity implementation. Based on our performance analysis, NM-SpMM employs a hierarchical blocking mechanism as a general optimization to enhance data locality, while memory access optimization and pipeline design are introduced as sparsity-aware optimization, allowing it to achieve close-to-theoretical peak performance across different sparsity levels. Experimental results show that NM-SpMM is 2.1x faster than nmSPARSE (the state-of-the-art for general $N:M$ sparsity) and 1.4x to 6.3x faster than cuBLAS’s dense GEMM operations, closely approaching the theoretical maximum speedup resulting from the reduction in computation due to sparsity. NM-SpMM is open source and publicly available at <https://github.com/M-H482/NM-SpMM>.

Index Terms— $N:M$ sparsity, GPU, Performance Optimization

I. INTRODUCTION

Deep learning, especially large language models (LLMs), demonstrates effectiveness across a wide range of tasks, including computer vision, natural language processing, knowledge representation, recommendation systems, drug discovery, and more [1]–[5]. However, artificial deep learning models are traditionally dense and over-parameterized [6]–[8], leading to significant consumption of computing and memory resources during actual real-world deployment. To address this issue, weight pruning serves as an effective strategy for reducing the size of deep learning models by eliminating less relevant weight elements while maintaining model accuracy [9]–[12]. $N:M$ sparsity matrix multiplication is the most performant solution in the weight pruning field, where dense matrix

multiplications in the model are converted into semi-sparse matrix multiplications [8], [13], [14].

The optimization of $N:M$ sparsity matrix multiplication is motivated by the increasing scale of artificial intelligence models in the real world, which leads to a higher demand for model inference to use pruning to reduce computation, memory, and latency [15]–[17]. Sparsity-based pruning improves model performance by reducing computational workload and memory usage, but also leads to accuracy loss [8]. The $N:M$ sparsity provides an option for balancing performance and model accuracy [18], but introduces more complex programming and optimization challenges. The goal of our work NM-SpMM is to achieve superior performance compared to state-of-the-art methods across various sparsity levels with systematic performance analysis.

There are three major challenges in the implementation of NM-SpMM: 1) Flexibility on $N:M$ sparsity: Existing works support only a restricted set of $N:M$ ratios [18], or confined to specific architectures [19], [20], or overly complex designs which hard to implementation [21]. To that end, we adopt a vector-based $N:M$ sparsity pattern, retaining a pattern of N vectors for every M vectors and supports multiple vector length. This approach allows for easy integration with front-end Python APIs and also enables more selectable pruning sparsity. 2) Lack of performance analysis: As we support more sparsity options, variation in sparsity affects the performance bottleneck from a computational bottleneck to a memory access bottleneck. To that end, we design a systematic top-down performance analysis model for $N:M$ sparsity. We calculate the arithmetic intensity (AI) of $N:M$ sparsity matrix multiplication across various matrix shapes and sparsity levels, and combine with roofline model to determine its optimization direction. 3) Low efficiency: How to select the optimal method with our performance analysis, to achieve close-to-theoretical peak performance across a wide range of sparsity levels become the final challenge.

To fix the above challenge issues, this work involves two

steps: Firstly, general optimization based on dense matrix multiplication. We adapt dense GEMM optimization, such as blocking to enhance data locality and reordering to avoid bank conflict, to $N:M$ sparsity matrix multiplication. Secondly, we propose sparsity-aware optimization for different sparsity levels. Specially in practice, for matrix with moderate sparsity, in computational bound, we orchestration arrange instruction pipeline so that FMA instructions cover load instructions as much as possible. For high-sparsity matrix, in memory bound, we minimize the memory footprint and use load instructions to overlap FMA instructions in the pipeline.

Overall, the contributions of this paper are as follows:

- NM-SpMM supports flexible $N:M$ ratios without dependence on specific hardware. It adopts a simple sparse pattern, retaining N vectors for every M vectors, facilitating its integration with algorithm research.
- We detail the anatomy of the $N:M$ sparsity computation bottleneck, revealing its transition from a computing bound to a memory bound as sparsity increases. This common characteristic aids in optimizing $N:M$ sparsity computation on other platforms.
- We propose general optimization that provide data locality through a hierarchical blocking mechanism, along with sparsity-aware optimization that reduce memory footprint and enhance pipeline design.
- We implement our approach effectively, with experimental results showing that our performance is 2.1x faster than nmSPARSE and 1.4x to 6.3x faster than cuBLAS’s dense GEMM operations.

The rest of this paper is organized as follows: Section II provides a brief introduction to $N:M$ sparsity and related work. Section III begins with a systematic analysis and introduces the optimization process step by step. The evaluated results and performance discussion are presented in Section IV. Finally, Section VI concludes this work.

II. BACKGROUND

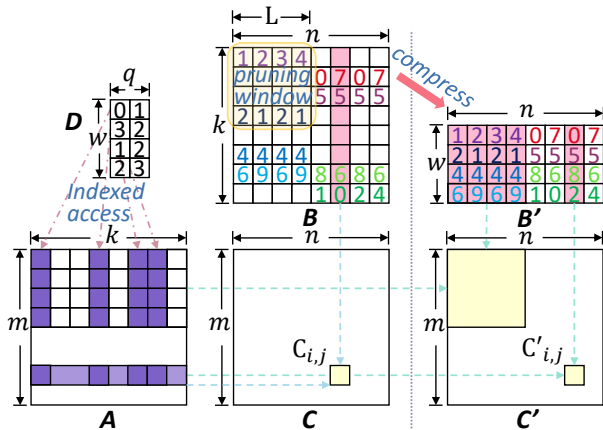


Fig. 1: An example demonstrates how vector-wise $N:M$ sparsity works, where $N = 2$, $M = 4$, and the vector length $L = 4$.

A. $N:M$ Sparsity Computation

To accelerate dense matrix multiplication $A = B \times C$, we utilize $N:M$ sparsity to prune matrix B , where A , B , and C have dimensions $m \times k$, $k \times n$, and $m \times n$, respectively. $N:M$ sparsity retains N units within every M consecutive pruning units. This paper focuses on optimizing $N:M$ sparsity using vector as pruning unit. In Figure 1, we select N vectors from every M vector along the k dimension of matrix B , depicted as a light yellow square frame. The selected N vectors are stored in a compressed matrix B' (shown in the blue box). An index matrix D of shape $w \times q$ stores the indices of the selected N vectors within each pruning window of matrix B , where $w = \lceil \frac{k \cdot N}{M} \rceil$ and $q = \lceil \frac{n}{L} \rceil$. We assume k is divisible by M and n by L ; otherwise, padding is applied, resulting in $w = \frac{k \cdot N}{M}$ and $q = \frac{n}{L}$. Finally we get the result matrix C' to approximating the original result matrix C with a confusion matrix W :

$$C'[i][j] = \frac{M}{N} \cdot \sum_{u=0}^w A[i][\frac{uM}{N} + D[u][\frac{j}{L}]] \cdot B'[u][j] \quad (1)$$

$$W[i][j] = \frac{|C'[i][j] - C[i][j]|}{m \cdot n} \quad (2)$$

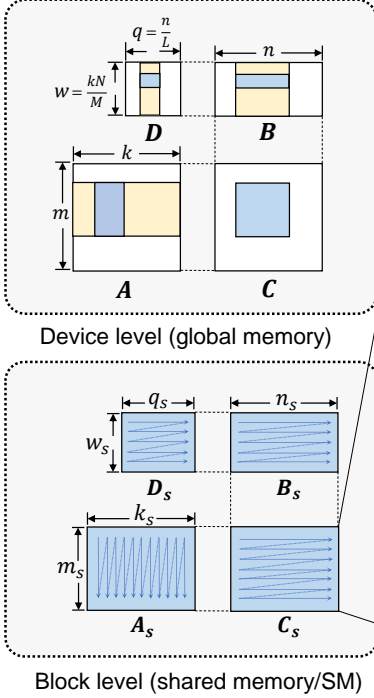
For convenience, we redefine the operation in equation 1 as $C = A \otimes (B, D)$. From the equations above, we conclude that: 1) computation operations are reduced to a ratio of $\frac{N}{M}$; 2) the same proportion of memory access on B is saved, with additional data access required for matrix D ; 3) this creates optimization opportunity for the indirect data access pattern in matrix A .

B. Related Works

Previous research on $N:M$ sparsity focuses on two categories: 1) $N:M$ sparsity implementation and optimization; 2) maintaining accuracy for sparse network.

$N:M$ sparsity implementation and optimization: NVIDIA [18] introduces Sparse Tensor Cores in the Ampere GPU architecture [22], using a 2:4 element-wise sparsity pattern to double the math throughput of dense Tensor Cores. Castro et al. [19] introduces the $V:N:M$ format and Spatha sparse library, enabling arbitrary $N:M$ ratios on Sparse Tensor Cores. However, Spatha’s two-stage pruning creates a pattern distinct from the $N:M$ sparsity studied in the algorithm community, making it incompatible with algorithms designed to preserve $N:M$ sparse network accuracy. Recent studies [23]–[30] show that vector-wise or block-wise sparse patterns offer significant performance benefits on modern general-purpose hardware by enhancing data reuse in L1 cache and registers. Lin et al. [31] propose nmSPARSE, which combines $N:M$ sparsity with vector-wise and block-wise pruning to support arbitrary $N:M$ ratios, eliminating the need for Sparse Tensor Cores. But, the nmSPARSE remains sub-optimal as it does not fully exploit the locality introduced by $N:M$ sparsity or optimize for different sparsity levels. Additionally, there are $N:M$ sparsity accelerators designed for specific network or pruning algorithm [20], [21].

III-B. Hierarchical Blocking Mechanism



III-C. Sparsity-Aware Optimization

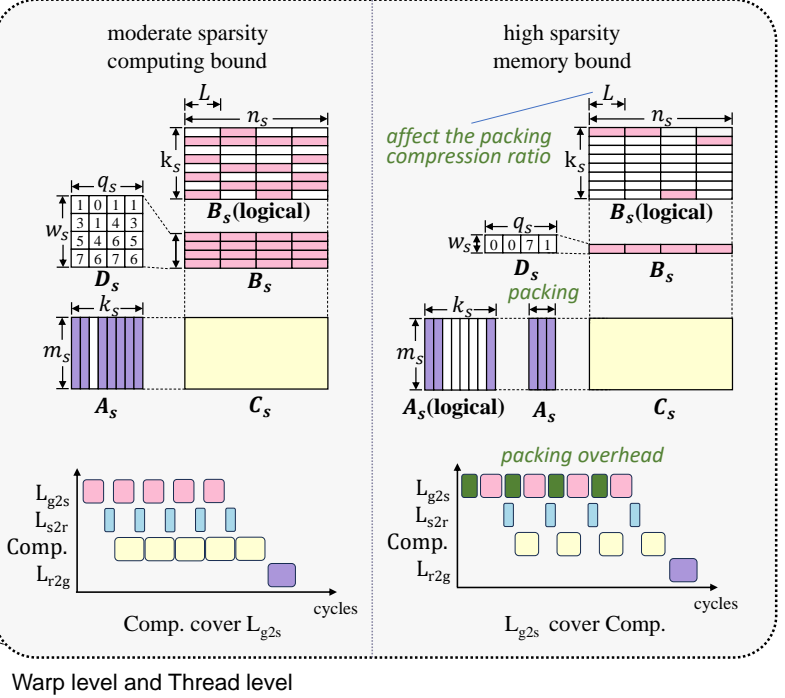


Fig. 2: Overview of the Workflow and Internals of NM-SpMM.

Maintaining accuracy for sparse network: With the emergence of Sparse Tensor Cores, a large amount of research focuses on how to improve the accuracy of $N:M$ sparse networks. Our work follows the naive $N:M$ pattern, so we can combine it with these works to jointly promote the application of sparse networks. NVIDIA [22] introduces $N:M$ sparsity to accelerate inference using a standard three-step pipeline: pre-training, pruning, and fine-tuning. Pool et al. [32] enhance accuracy with channel permutation, while Sun et al. [33], [34] propose a layer-wise $N:M$ scheme for improved precision over uniform sparsity. Efforts to optimize $N:M$ training efficiency include Zhou et al.’s regularization term for learning sparsity [35], Hubara et al.’s transposable masks for faster backward passes [36], and Zhang et al.’s Bi-Mask [37]. Extensions like applying $N:M$ to activations [38], combinatorial approaches [39], and adaptive mask learning [40] further enhance training efficiency. Xiang et al. [41] introduce the MaxQ method for incrementally applying sparsity during training.

III. METHOD

The whole optimization workflow of NM-SpMM is illustrated in Figure 2. Specifically, it includes a hierarchical blocking mechanism and sparsity-aware optimization. In Section III-A, we first provide a systematic analysis of the $N:M$ sparsity computation, followed by a detailed introduction to the hierarchical blocking mechanism and sparsity-aware optimization in Section III-B and Section III-C, respectively.

A. Analysis of Optimization Strategies for $N:M$ Sparsity Computation

In this subsection, we first briefly introduce how we analyze the $N:M$ sparsity computation pattern and provide an overview of the optimization process, while outlining the key factors that influence performance. Then, in the following subsections, we provide a detailed step-by-step explanation of our optimization approach.

The input to the $N:M$ sparsity computation problem consists of two matrices, A and B , with dimensions $m \times k$ and $w \times n$, respectively. Matrix B is compressed using the method shown in Figure 1, as well as the N and M configuration is adjusted to accommodate different sparsity levels.

First, we use a **hierarchical blocking mechanism that adapts to the GPU’s storage architecture to enhance data locality**. Because the $N:M$ sparsity pattern resolves load imbalance problem in sparse matrix multiplication, the fine-grained data locality achieved by using vector as pruning unit eliminates irregular memory access issues. Therefore, we can design the blocking method based on the optimization strategies used in dense matrix multiplication. However, the hierarchical blocking mechanism introduces several parameter configurations, including matrix size parameters for shared memory blocking (m_s, n_s, k_s, w_s, q_s), register blocking parameters (m_t, n_t), and parameters affecting warp instruction scheduling (m_r, n_r), as shown in Figure 3. The parameters m_s, n_s, k_s , and w_s are constrained by the shared memory capacity on the Stream Multi-processor (SM), as indicated in

Equation 4. The block parameters at the warp level and thread level (m_t, n_t, m_r, n_r) impact the performance of the inner kernel. It is necessary to consider the number of registers used by each thread, as well as the compute-to-memory access ratio of the inner kernel. This is influenced by warp-level analysis, as the GPU uses warps as the scheduling units for instructions, and shared memory access is also evaluated at the warp level. The detailed analysis can be referenced in Section III-B, and for matrices of different input size, we provide recommended parameter configurations in Table I. For handling different sparsity levels (i.e., different N and M), we adaptively adjust the parameters based on the capacity of shared memory.

Another important point is that **varying degrees of sparsity will affect the computation pattern of $N:M$ sparsity**. As shown in Figure 2, we cache the sub-matrix A_s and B_s of matrix A and B in shared memory to reduce accesses to global memory. The sparsity is given by $1 - \frac{N}{M}$ or $1 - \frac{w_s}{k_s}$, where k_s is typically equal to M (or sometimes a multiple of M). In this paper, we define sparsity below 70.0% as moderate and above 70.0% as high. According to the roofline analyses and our experimental results, when the sparsity exceeds 70.0%, the performance bottleneck shifts. But the transition point varies depending on the arithmetic intensity of the hardware. We select four typical levels: 50.0%, 62.5%, 75.0%, and 87.5%. Based on the vector length L , B_s is divided into $\frac{n_s}{L}$ pruning windows (four in Figure 2) along the row direction. Within each pruning window, according to the rules of matrix multiplication, the pink vector from a specific row of B_s computes with the purple vector from the corresponding column in A_s .

One can see that the upper bound of the memory footprint of A_s is $m_s \times k_s$, while the lower bound is $m_s \times w_s$. The memory footprint of A_s is influenced by both sparsity and vector length. Lower sparsity results in a larger memory footprint within each pruning window, while a smaller vector length L leads to more pruning windows along the row direction of B_s , thereby increasing the combined memory footprint of multiple pruning windows. Additionally, as L decreases, the accuracy of the $N:M$ sparse network improves, while a larger L facilitates load distribution within the warp and data reuse within a thread, resulting in a more efficient inner kernel. As shown in Figure 2, in the cases of moderate sparsity and high sparsity, the memory footprint of A_s accounts for 7/8 and 3/8 of the working set (memory address space to be accessed), respectively. In contrast, B_s is stored in a compressed format, with a fixed memory footprint of $w_s \times n_s$. The memory footprint of D_s is relatively small and can be ignored. The computational workload for $C_s = A_s \otimes (B_s, D_s)$ is $2 \times m_s \times n_s \times w_s$. Therefore, the arithmetic intensity of $N:M$ sparsity can be expressed as:

$$AI = \frac{2 \cdot m_s \cdot n_s \cdot w_s}{m_s \cdot k_s + w_s \cdot n_s + 2 \cdot m_s \cdot n_s} \quad (3)$$

From Equation 3, we can conclude that as sparsity increases, the arithmetic intensity decreases. This is because, given that $w_s = k_s \cdot (1 - \text{sparsity})$, the numerator decreases with increasing sparsity, while in the denominator, only the operand

$w_s \cdot n_s$ decreases proportionally. Therefore, the overall fraction decreases. In summary, in the moderate sparsity scenario, the working set of A_s is almost fully utilized, making the $N:M$ sparsity computation more computing bound. In contrast, in the high sparsity scenario, as sparsity increases, both the computational workload and the memory footprint of B_s decrease proportionally, while the memory footprint of A_s does not reduce at the same rate, resulting in a memory bound computation.

Therefore, due to the different computational characteristics in various sparsity scenarios, we propose sparsity-aware optimization: memory access design for footprint minimization and pipeline design for instruction latency hiding. In briefly, for the computing bound problem in the moderate sparsity scenario, we load A_s using a non-packing approach. For the memory bound problem in the high sparsity scenario, we first obtain information about the valid data needed in each block of A_s through offline processing (marked as *col_info*). During online computation, we then pack A_s using *col_info* to reduce the memory footprint.

Then, we design pipelines for both scenarios to hide instruction latency. In the moderate sparsity scenario, we design the pipeline to use computation instructions to mask the instruction latency from loading data from global memory to shared memory. In the high sparsity scenario, due to packing requiring *col_info* to be loaded from global memory first, we use the instructions for loading data from global memory to shared memory to mitigate the latency of computation instructions. Additionally, in the inner kernel, we minimize the indirect memory access impact caused by $N:M$ sparsity through pre-fetching. For more details, please refer to Section III-C.

B. Hierarchical Blocking Mechanism

1) *Blocking for SM Shared Memory*: Each Streaming Multiprocessor (SM) in GPGPU is configured with a shared memory on the chip with lower access latency compared to its global memory. Thus, to improve data locality, we first block the input matrices $A[m][k]$, $B[w][n]$, and $D[w][q]$ into smaller blocks, denoted $A_s[m_s][k_s]$, $B_s[w_s][n_s]$, and $D_s[w_s][q_s]$, as shown in the top-left corner of Figure 3. Note that $w_s = \frac{k_s \cdot N}{M}$, $q_s = \frac{n_s}{L}$. Each thread block loads A_s , B_s and D_s into shared memory on each SM to compute C_s , this is illustrated in Figure top-right corner of 3. In this blocking process, the block size of these three matrices is **limited by the memory size of the SM shared memory**. Thus the block size parameters must satisfy the equation below:

$$4 \cdot (k_s \cdot m_s + w_s \cdot n_s + w_s \cdot q_s) \leq SM_Size * 0.5 \quad (4)$$

Here SM_Size denotes the shared memory size on each SM. We keep half of its shared memory for buffering and other temporary variable. Since the index matrix D only needs to provide the position of each retained vector within the pruning window, each element requires only $\log_2 M$ bits. Thus we

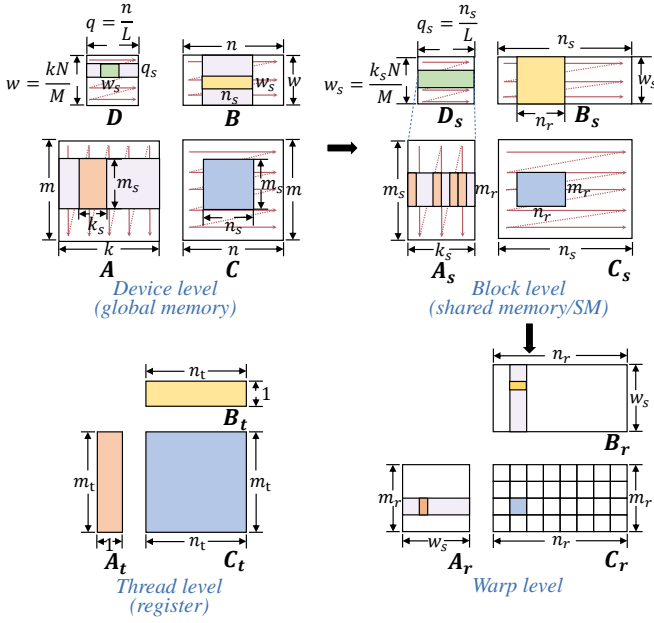


Fig. 3: A hierarchical pipeline of the NM-SpMM GPU implementation.

Listing 1: Blocking algorithm for SM shared memory.

```

1  __global__ void NM-SpMM(float A[m][k], float B[w
2  ][n], float D[w][q], float C[m][n]) {
3  //Calculate the block size for A_s, B_s, D_s
4  (m_s, n_s, m_t, n_t) = Para_Init_Table(m, n);
5  k_s = min(k, (M * SM_Size) / (8 * (N * m_s + N * n_s)));
6  w_s = k_s * N / M, q_s = n_s / L;
7  //Allocate shared memory for A_s, B_s, D_s
8  __shared__ float A_s[m_s][k_s], B_s[w_s][n_s], D_s[w_s
9  ][q_s];
10 //Allocate accumulator registers
11 float C_t[m_t][n_t] = {0};
12 //Calculate the offset for each block
13 int b_i = blockIdx.y * m_s;
14 int b_j = blockIdx.x * n_s;
15 // Main loop
16 for(int u = 0; u < w; u = u + w_s) {
17 //Load blocks from global to shared memory
18 A_s = LoadTile(A, b_i, u, k, k_s, m_s);
19 B_s = LoadTile(B, b_j, u, n, w_s, n_s);
20 D_s = LoadTile(D, b_j, u, w, w_s, q_s);
21 //Synchronization after data loading
22 __syncthreads();
23 SMBlock(A_s, B_s, D_s, C_t, w_s, m_t, n_t);
24 //Synchronization after computation
25 __syncthreads();
26 }
27 //Store the results C_t back to global memory
28 StoreFrag(C, C_t);

```

ignore the shared memory size used by $D_s[w_s][q_s]$ to simplify equation 4, then we can update equation 4 to be:

$$8 \cdot k_s(m_s + \frac{N \cdot n_s}{M}) \leq SM_Size \quad (5)$$

We also need to **maximize the block-level arithmetic intensity**, as shown in Equation 3. The actual value for m_s and n_s are the user-defined parameter settings. Different settings

are selected based on the size of the input matrix size, some recommended configurations for m_s and n_s are given in Table I to accommodate small, medium and large matrices. **To avoid bank conflict in shared memory access, m_s and n_s are set as multiples of 32.** Once the values of m_s and n_s are determined, the maximum k_s can be directly calculated using Equation 4, as **a larger k_s ensures sufficient compute instructions in the pipeline of inner kernel.**

	m_s	n_s	m_r	n_r	m_t	n_t
small	32	32	16	32	4	4
medium	32	64	32	32	8	4
large	64	128	64	32	8	8

TABLE I: Recommended parameter configurations for SM shared memory blocking, warp-level tiling and thread tiling.

We demonstrate this blocking process in Listing 1. In line 3, we first initiate the blocking parameters m_s, n_s, m_t, n_t using the configurations given by Table I. k_s are calculated with the formula given by equation 4 in line 4. Then line 7 declares and allocates the SM shared memory space for A_s, B_s , and D_s . We also assign a temporary matrix $C_t[m_t][n_t]$ as a result accumulator and initialize it with zeros. The offset for each block is calculated by lines 11 to 12. We loop over the k_s and w_s dimension with a step k_s and w_s respectively between lines 14 to 24. In each iteration A_s, B_s , and D_s are loaded into shared memory, then the function *SMBlock* is routed to calculate the sub-problem. Finally, the accumulated result is saved back to global memory in line 26.

The following subsection introduce how we implement the function *SMBlock*, and to fully utilize the registers, we tiling each block again to fit each tile into the registers and dispatch the workload to each thread hosting one FP32 ALU.

2) Warp Tiling for Thread Inner Kernel Optimization:

Blocks from the above subsection are sent to each SM for calculation, a further warp tiling method is needed to dispatch the workload to multiple warps (or a cluster of threads). NVIDIA GPUs are configured with hundreds of SMs. Each SM utilizes a single-instruction multiple-thread (SIMT) programming model and can simultaneously launch up to 64 warps on the A100. Each warp consists of 32 threads, and the thread arrangement within a warp is performance sensitive. A warp with 32 threads can be arranged in a grid of $x \times y$, for example $1 \times 32, 2 \times 16, 4 \times 8, 8 \times 4$, etc. The more square grid 4×8 or 8×4 are better in most cases. Figure 3 (bottom left) illustrates an example with a 4×8 grid, where the 8 threads in each row access different banks of B_s and broadcast to the 4 threads in the corresponding column. 32 threads in a wrap are scheduled out-of-order in parallel to one stream processor (SP), and only 16 threads can be executed simultaneously, for each SP has only 16 FP32 cores.

The arithmetic intensity of the inner kernel executed by each thread is crucial for achieving high computation efficiency. Since each thread runs on a physical FP32 core and is limited to 255 registers, we aim to **maximize the computing-to-memory-access ratio (CMAR) of the inner kernel** to

Listing 2: Warp tiling algorithm with thread inner-kernel optimization.

```

1  __device__ void SMBlock(float As[ks][ms], float Bs
   [ws][ns], float Ds[ws][qs], float Ct[mt][nt],
   int ws, int mt, int nt){
2  // Allocate register buffer
3  float At[mt], Bt[nt];
4  // Calculate the offset of Warp tile
5  int ti, tj;
6  ThreadIndexing(ti, tj, mt, nt);
7  // SM block loop
8  for(int p = 0; p < ws; p++){
9  // Load At, Bt from shared memory to register
10  At=LoadFragByIdx(As, ti, p, Ds);
11  Bt=LoadFrag(Bs, tj, p);
12  // Calculate the outer product of At and Bt
13  InnerKernel(At, Bt, Ct, mt, nt);
14  }
15 }
16
17 __device__ void ThreadIndexing(int& ti, int& tj,
   int mt, int nt){
18  int tid = threadIdx.y*blockDim.x + threadIdx.x;
19  int warp_id = tid / warpSize;
20  int lane_id = tid % warpSize;
21  // Arrange the threads in a warp into a 4x8 grid
22  ti = warp_id/2 * mt * 4 + lane_id/8 * mt;
23  tj = warp_id%2 * nt * 8 + lane_id%8 * nt;
24  }
25
26 __device__ void InnerKernel(float At[mt], float Bt
   [nt], float Ct[mt][nt], int mt, int nt){
27  // Calculate the outer product of At and Bt
28  for(int i = 0; i < mt; i++){
29  for(int j = 0; j < nt; j++){
30  Ct[i][j] += At[i] * Bt[j];
31  }
32  }
33 }

```

optimize performance. We first extract compressed columns from A_s with the indices provided by D_s to form a new matrix A_r during warp tiling. Then the innermost computation for the thread transforms into a general matrix multiplication (GEMM). To maximize CMAR, we will increase the FP32 FMA instructions to LDS (load from shared memory) instructions for each thread’s inner kernel while ensuring that there are no bank conflict. Therefore, a thread tiling is applied with a thread tile of size $m_t \times n_t$, the number of FMA instructions in the thread block is $m_t \times n_t$, and the number of LDS instructions is proportional to the sum of m_t and n_t (with the proportionality constant α , which depends on the LDS access width, such as $\alpha = 4$ in LDS.32, $\alpha = 2$ in LDS.64, and $\alpha = 1$ in LDS.128). Thread block size should satisfy $(m_t + n_t + m_t \cdot n_t) \leq 255$, where 255 refers to the maximum number of registers available per thread. Because **using too many registers per thread reduces parallelism**, which is referred to as occupancy in NVIDIA GPUs. Under this constraint, the CMAR is maximized:

$$CMAR = \frac{1}{\alpha} \cdot \frac{m_t \cdot n_t}{m_t + n_t} \quad (6)$$

One can see that the larger m_t and n_t are, the higher the CMAR is. On A100, m_t and n_t are typically set to 8×8 or 8×16 . For small matrices, using a smaller thread tile size, such as 8×4 or 4×4 , reduces the resource usage per thread. This

allows more threads to be launched simultaneously, thereby increasing occupancy and improving computational efficiency.

The Warp tiling algorithm and thread inner kernel optimization are presented in Listing 2 and Figure 3 (bottom left). We first allocate registers for A_t and B_t to load data for thread inner kernel in line 3. Then the thread index is calculated by the function *ThreadIndexing* in line 6. The implementation of the function *ThreadIndexing* is presented from line 17 to line 24, and here we provide an example of its implementation using grid 4×8 . After that, each thread loads A_t , B_t into registers for computation with thread *InnerKernel* function. Its detailed implementation is presented from line 26 to line 33. Finally the results C_t are accumulated in the registers before being written back to C in global memory.

C. Sparsity-Aware Optimization

1) Memory Access Design for Footprint Minimization:

In Section III-A, we explore how different levels of sparsity impact the computation pattern, emphasizing the distinctions between moderate and high sparsity. As a result, we propose packing strategy to address the high sparsity scenario and non-packing strategy to resolve the moderate sparsity scenario.

We design a packing approach to minimize the memory footprint of matrix A_s and eliminate redundant reads of matrix A in high sparsity scenarios. For example, packing can reduce the global memory access of A_s to $\frac{n_s \cdot N}{L \cdot M}$, where $\frac{n_s}{L}$ represents the number of pruning window per row in B_s . When the pattern of each pruning window is identical, the memory access minimize to $\frac{N}{M}$. Specifically, we conduct offline pre-processing to accomplish three tasks. First, we identify the necessary columns in A_s , referred to as *col_info*. Second, we reorder the index matrix D to establish the mapping for $N:M$ sparsity. Third, we transform the data layout of matrix D to reduce the number of global memory transactions. The offline pre-processing procedure is shown in Figure 4 and Listing 3 lines 2-6. During computation, we online pack A_s by *col_info* to reduce memory footprint and increase arithmetic intensity. Before loading A_s , we first load *col_info* from global memory, which increases latency. In Section III-C2, we design a refined pipeline to mask this latency. The *col_info* introduces an additional 1% to 10% GPU memory overhead, calculated as $\frac{k_s - q_s}{w_s \cdot q_s} \%$ of D_s , which is negligible in practice.

The non-packing strategy directly loads the entire working set of A_s into shared memory for moderate sparsity scenarios in an ostrich-style approach. For moderate sparsity scenarios, the valid data in A_s occupies the majority of its working set. Therefore, non-packing does not cause redundant reads, and skipping packing avoids the overhead of pre-processing and reading *col_info*. There are two main reasons for the high proportion of effective data in A_s in the scenario of moderate sparsity: a) When sparsity is moderate, the proportion of valid data within a single pruning window is relatively high. b) For both $N:M$ sparse network accuracy and computational efficiency considerations, there are multiple pruning windows in the row direction of B_s , each often with a different pattern, as shown in Figure 2. As shown in Listing 3 lines 13-

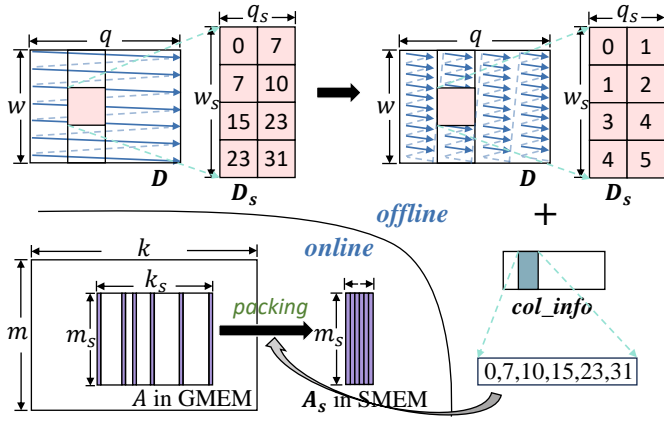


Fig. 4: Offline pre-processing of the index matrix in high sparsity scenarios: obtaining *col_info*, rearranging indices, and changing the data layout. During computation, online packing of A_s reduces memory footprint and enhances arithmetic intensity.

Listing 3: NM-SpM²M with sparsity-aware optimization to reduce memory footprint.

```

1 // Offline init when sparsity is high
2 void PreProcessing(float A[m][k], float B[w][n],
3   float D[w][q]) {
4   col_info = queryColInfo(D, w_s, q_s);
5   D = reoderingIdx(D, w_s, q_s, col_info);
6   D = transformLayout(D, w_s, q_s);
7 }
8
9 __global__ void NM-SpM2M(float A[m][k], float B[w][n],
10  float D[w][q], int* col_info, float C[m][n]) {
11  ...
12  __shared__ int sh_col_info[k_s];
13  // Main loop
14  for(int u = 0; u < w; u = u + w_s) {
15    // Load SM Block from global memory to shared
16    // memory
17    if(sparsity > threshold) {
18      // packing load
19      sh_col_info = loadColInfo(col_info, b_j, u);
20      __syncthreads();
21      A_s = LoadTileByColInfo(A, b_i, u, sh_col_info);
22    } else {
23      // non-packing load
24      A_s = LoadTile(A, b_i, u);
25    }
26    B_s = LoadTile(B, b_j, u);
27    D_s = LoadTile(D, b_j, u);
28    // Synchronization for data loading
29    __syncthreads();
30    SMBlock(A_s, B_s, D_s, C_t, w_s, m_t, n_t);
31    // Synchronization for computation completion
32    __syncthreads();
33  }
34  // Write result to global memory
35  StoreFrag(C, C_t, b_i + t_i, b_j + t_j);
36 }

```

21, for high sparsity scenarios, we use a packing strategy to avoid redundant global memory accesses. For moderate sparsity scenarios, we load the data directly without packing for efficiency.

2) *Pipeline Design for Instruction Latency Hiding*: In Section III-B, we leverage data locality provided by the hierarchi-

cal blocking mechanism to accelerate computation. In Section III-C, we perform sparsity-aware memory access optimization at the thread block level. However, in Listing 3, there are still load-compute and load-load dependencies that prevent the compute units from being fully utilized. Specifically, load-compute dependencies occur between loading A_s , B_s , and D_s , or A_t and B_t and the subsequent computation. Load-load dependencies occur between loading *col_info* and loading A_s , as well as between reading indices from D_s and loading A_t .

We design pipelines for high sparsity and moderate sparsity to break these two dependencies, thereby hiding instruction latency and enhancing instruction-level parallelism while improving hardware utilization. In the hierarchical blocking mechanism, a large number of registers are used to accumulate C_t , resulting in lower occupancy and limited potential for increasing thread-level parallelism. The key to using pipelines to hide instruction latency is identifying which set of instructions can mask the latency of another set. Based on the analysis in Section III-A, in the moderate sparsity scenario, we use computation instructions to mask the latency of data transfer instructions from global memory to shared memory, as shown in Figure 5. In contrast, in the high sparsity scenario, due to the overhead from packing and the inability to proportionally reduce the memory footprint of A_s , we utilize instructions that load data from global memory to shared memory to hide the latency of computation instructions, as illustrated in 6.

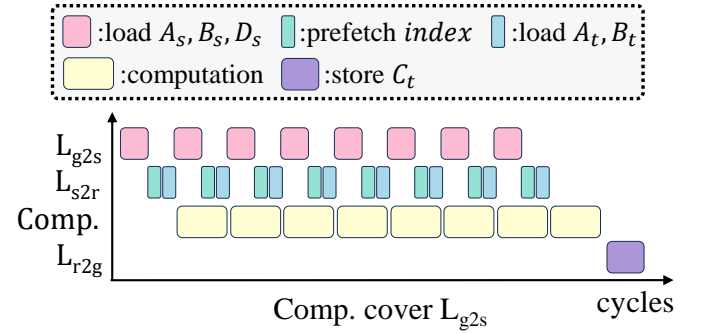


Fig. 5: Pipeline of NM-SpM²M for moderate sparsity scenario: utilizing computation instructions to mask latency of load instructions from global memory to shared memory.

Specifically, we utilize double buffering to achieve overlap between different types of instructions. Therefore, in Listing 4, we allocate double the buffer space (line 4,31), computing on data from one buffer while writing the next round data to the other buffer. In Listing 4, lines 14 to 24 contain the main loop, where line 17 loads the next round of the SM block, line 19 performs computations based on the current SM block, and line 20 waits for data loading to complete. Outside the main loop, line 10 is responsible for loading the first SM block, and line 26 computes the final SM block. The *SMBlock* function follows a similar logic: lines 39-40 read data for the next warp tiling, line 42 performs computations on the current warp tiling, and lines 34-35 and 45 handle the processing of the first and final warp tiling, respectively. Unlike previously,

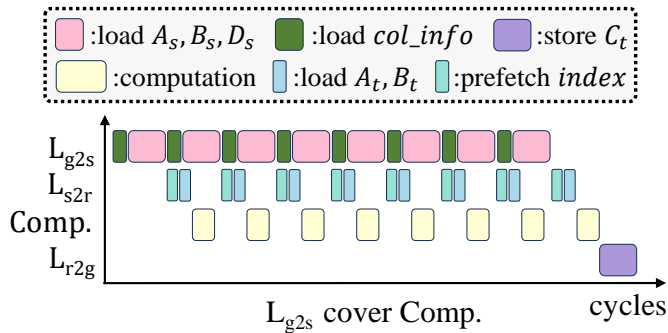


Fig. 6: Pipeline of NM-SpMM for high sparsity scenario: employing instructions for loading data from global memory into shared memory to hide latency of computation instructions.

there are no explicit asynchronous instructions required in this case. By issuing shared memory access instructions prior to the computation instructions, we enable the overlap of data transfer from shared memory to registers with computation, as illustrated by the blue and yellow rectangles in Figure 5. To avoid excessive shared memory access instructions in the inner kernel, we pre-fetch the indices required by each thread from shared memory (D_s) into registers, as shown in Listing 4 lines 12 and 23. This enhances the computation-to-memory access ratio in the inner kernel.

IV. PERFORMANCE EVALUATION

A. Datasets and Evaluation Environments

Our dataset consists of 100 data points. These data points are extracted from linear layers in Llama [5] models. In detail, the input sequence m ranges from 2^8 to 2^{12} , yielding five distinct values. Each value is associated with 20 data points, where the tuples (n, k) are extracted from the Llama model. Then there are 100 combinations of (m, n, k) in our dataset. In addition, to validate the kernels we design for small, medium, and large matrices (see Table I), we select several small, medium, and large input matrices as test cases, as shown in Table II.

Our evaluation environments include three GPU cards: one NVIDIA A100 80GB PCIe, one NVIDIA RTX 3090, and one NVIDIA RTX 4090. Some key parameters of these three GPUs are shown in Table III. The operating system on our test is CentOS 7.9 with CUDA 12.2. We implement our work using C++ and CUDA, and name it **NM-SpMM**. NM-SpMM is compared with all state-of-the-art dense and sparse libraries, including cuBLAS (a vendor-specific library for dense matrix computation by NVIDIA), nmSPARSE [31] (a state-of-the-art library of general $N:M$ sparsity implementation), and Sputnik [42] (an excellent library of sparse linear algebra kernels for deep learning). Without loss of generality, four typical sparsity ratios—50.0%, 62.5%, 75.0%, and 87.5%—are used in our benchmark evaluations.

Listing 4: NM-SpMM with sparsity-aware optimization to hide instruction latency.

```

1  __global__ void NM-SpMM(float A[m][k], float B[w][
2  n], float D[w][q], int *col_info, float C[m][n]) {
3  ...
4  // Allocate double buffer
5  __shared__ float As[2][ks][ms], Bs[2][ws][ns],
6  Ds[2][ws][qs], col_info[2][ks];
7  float Ct[mt][nt]={0};
8  // Buffer for prefetching indices
9  int idx[ws];
10 int cur = 1, nex = 0;
11 // Load the first SM Block
12 LoadTile(A, B, D, As, Bs, Ds, bi, bj, 0, cur);
13 // Prefetch indices to register
14 idx = prefetch(Ds, 0, bj);
15 // Main loop
16 for(int u = ws; u < w; u = u + ws) {
17   cur = cur ^ 1, nex = nex ^ 1;
18   // Load the next SM block async
19   LoadTileAsync(A, B, D, As, Bs, Ds, bi, bj, u,
20     nex);
21   // Compute on the cur SM block
22   SMBlock(As[cur], Bs[cur], idx, Ct, ws, mt, nt);
23   WaitAsyncCopy();
24   __syncthreads();
25   // Prefetch indices to register
26   idx = prefetch(Ds, u, bj);
27 }
28 // Compute on the last SM block
29 SMBlock(As[cur^1], Bs[cur^1], idx, Ct, ws, mt, nt);
30 // Write result to global memory
31 StoreFrag(C, Ct, bi + ti, bj + tj);
32 }
33 device__ void SMBlock(float As[ks][ms], float Bs
34 [ws][ns], int idx[ws], float Ct[mt][nt], int ws,
35 int mt, int nt) {
36   float At[2][mt], Bt[2][nt]; int ti, tj;
37   ThreadIndexing(ti, tj);
38   // Load the first warp tiling
39   At[0] = LoadFragByIdxInReg(As, ti, 0, idx);
40   Bt[0] = LoadFrag(Bs, tj, 0);
41   // SM block loop
42   for(int p = 0; p < ws - 1; p = p + 1) {
43     // Load the next warp tiling
44     At[(p+1)%2] = LoadFragByIdxInReg(As, ti, p+1, idx);
45     Bt[(p+1)%2] = LoadFrag(Bs, tj, p+1);
46     // Compute on the cur warp tiling
47     InnerKernel(At[p%2], Bt[p%2], Ct, mt, nt);
48   }
49   // Compute on the last warp tiling
50   InnerKernel(At[1], Bt[1], Ct, mt, nt);
51 }

```

	small		medium		large	
label	A	B	C	D	E	F
m	512	512	512	1024	2048	4096
n	512	1024	2048	2048	4096	4096
k	512	1024	2048	2048	4096	4096

TABLE II: Examples of small, medium, and large matrices for evaluating kernels with different blocking parameters in Table I.

B. Evaluation on Step-wise Optimizations

The proposed step-wise optimizations in Section III are first evaluated for effectiveness. We name three versions for this experiment: V1 relates to the hierarchical blocking mechanism found in Listing 1 and Listing 2. In contrast, V2 focuses on the sparsity-aware memory footprint optimization presented in

Hardware Metric	A100 80G	RTX 3090	RTX 4090
Boost Clock (MHz)	1410	1695	2520
Peak FP32 TFLOPS	19.5	35.6	82.6
Number of SMs	108	82	128
Register File Size / SM (KB)	256	256	256
FP32 Cores / SM	64	128	128
FP32 FLOPs / clock / SM	128	256	256
L1 Data Cache / Shared Memory / SM (KB)	192	128	128
L2 Cache Size (MB)	40	6	72
Global Memory (DRAM) Size (GB)	80	24	24
DRAM Bandwidth (GB/s)	1935	936	1008

TABLE III: Hardware metrics comparison between A100 80G PCIe, RTX 3090, and RTX 4090 GPUs.

Listing 3. Lastly, V3 addresses the sparsity-aware instruction latency hiding optimization detailed in Listing 4. Each version incrementally builds on the previous one: V2 includes V1’s optimizations, and V3 encompasses both V1 and V2’s improvements.

In this experiment, square matrices with dimensions $m = n = k = 4096$ are used as our input data. We select four commonly used sparsity levels in deep learning: 50.0%, 62.5%, 75.0%, and 87.5%. In addition, there is a sparsity level of 0.0%, where our code sets $M = N = 32$, and cuBLAS performs dense matrix multiplication operations. As illustrated in Figure 7, we evaluate the efficiency of V1, V2, and V3 on three different GPUs: A100, 3090, and 4090.

When the sparsity is 0.0%, cuBLAS performs dense matrix multiplication, while NM-SpMm handles $N:M$ sparsity computation with both N and M set to 32. Through our optimizations, on A100, the computation of $N:M$ sparsity is comparable in efficiency to the cuBLAS dense matrix multiplication, indicating that the overhead of indirect memory access is well hidden. However, on the 3090 and 4090, the floating-point performance significantly outpaces memory bandwidth (see Table III), making it challenging to mask the overhead of indirect memory access.

When the sparsity is 50.0% or 62.5%, $N:M$ sparsity computations tend to be computing bound. The hierarchical blocking mechanism implemented in V1 provides good data locality, resulting in strong performance for V1, while subsequent versions show only minor improvements.

When the sparsity is 75% or 87.5%, $N:M$ sparsity computations become memory bound. The optimizations in V2 that reduce memory footprint, along with the pipeline optimizations in V3 that hide instruction latency, significantly enhance performance. For GPUs like the 3090 and 4090, where memory bandwidth is somewhat constrained relative to computational power, these optimizations targeting memory bound scenarios yield even more significant improvements.

C. Evaluation of Kernels with Different Blocking Parameters

In Section III-B, we propose a hierarchical blocking mechanism tailored to the characteristics of $N:M$ sparsity and provide

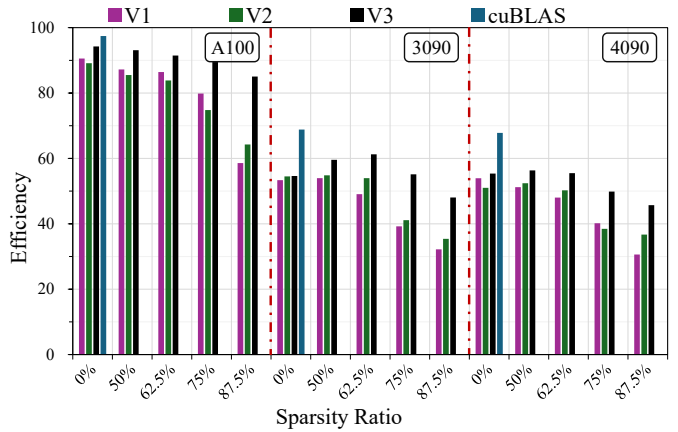


Fig. 7: Step-wise optimization evaluation of NM-SpMm on A100 with input matrix shape $m = n = k = 4096$.

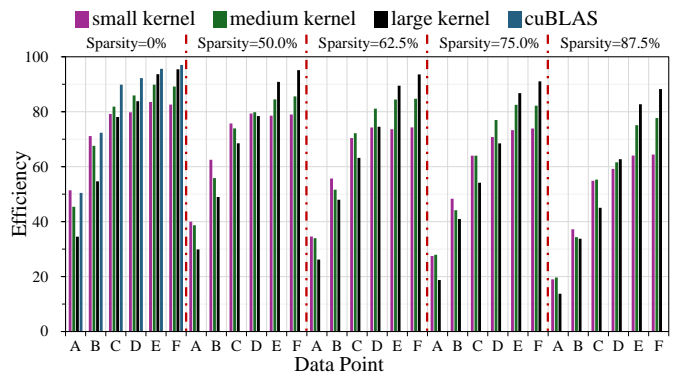


Fig. 8: Performance evaluation of kernels with different blocking parameters on A100. Detailed data points can be found in Table II.

recommended parameter configurations for small, medium, and large input matrices. As shown in Figure 8, the vertical axis represents efficiency, while the horizontal axis is divided into five regions corresponding to sparsity levels of 0.0%, 50.0%, 62.5%, 75.0%, and 87.5%. Each region contains six data points derived from the small, medium, and large matrices listed in Table II. The cuBLAS only appears when the sparsity level is 0.0%, as it can only perform dense GEMM operations.

At a sparsity level of 0.0%, our kernel nearly matches the performance of cuBLAS kernels across various input matrices of different size, even when accounting for the overhead of indirect memory access.

It is evident that, across all sparsity levels, kernels optimized for matrices with specific characteristics consistently achieve the best performance for those cases. For example, with smaller input matrices, the small kernel achieves the best performance, while the large kernel excels with larger matrices. This highlights both the effectiveness and necessity of designing kernels with different blocking parameters tailored to various matrix characteristics.

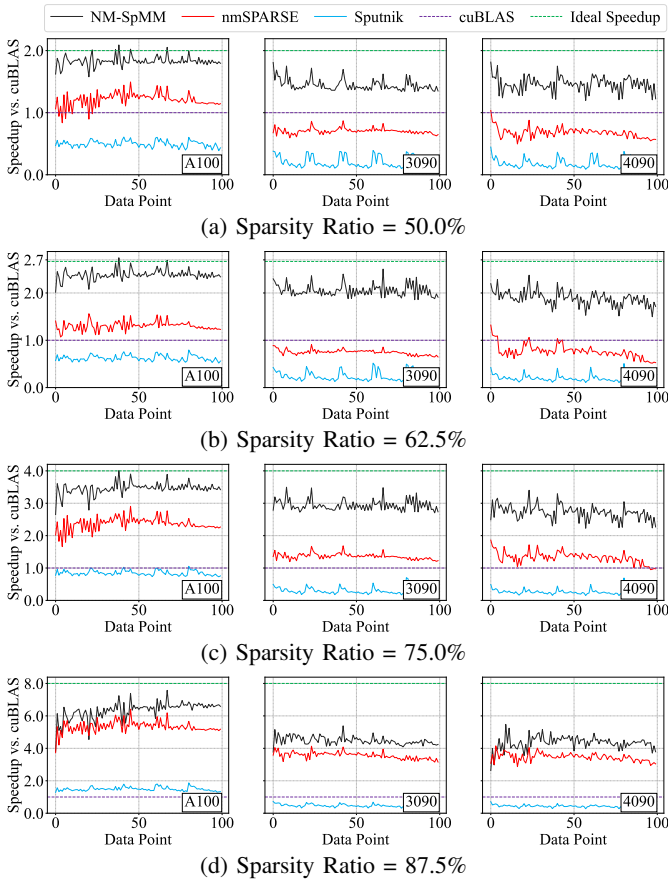


Fig. 9: Kernel performance On A100, 3090 and 4090.

D. Performance Evaluation with Related Works

In this experiment, we compare NM-SpMM with three other state-of-the-art works including cuBLAS, Sputnik, and nmSPARSE on three GPU cards. The data set used in these experiments contains 100 data points described previously. Again, four different sparsity levels, with two moderate sparsity and two high sparsity, are used. The evaluation results are illustrated in Figure 9.

In Figure 9, the vertical axis shows the speedup relative to cuBLAS dense computation, while the horizontal axis indicates the index of 100 data points. cuBLAS serves as a baseline, marked by a constant purple dashed line at 1 across all figures. The green dashed line represents the ideal speedup achievable with sparse matrices. For instance, with 75.0% sparsity, computation reduces to a quarter of the original, yielding an expected speedup of 4.

Similar trends are observed across various GPU cards, so we focus our analysis primarily on the data from the A100. The blue solid line represents Sputnik, which shows poorer performance due to its direct handling of unstructured sparse patterns, leading to irregular memory access and imbalanced workload overhead.

The nmSPARSE is denoted by a red solid line. It is a library designed specifically for $N:M$ sparsity. Compared to Sput-

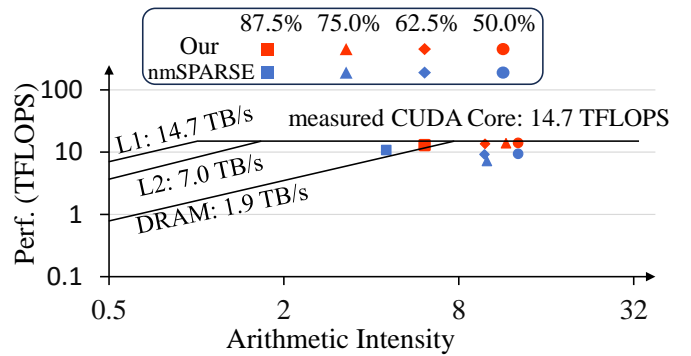


Fig. 10: Roofline analysis on A100, here $m = n = k = 4096$.

nik using an unstructured pattern, nmSPARSE demonstrates a significant performance advantage with its $N:M$ sparsity pattern. Therefore, nmSPARSE achieves speedups of about 1.2x, 1.3x, 2.4x, and 5.3x over cuBLAS at sparsity levels of 50.0%, 62.5%, 75.0%, and 87.5%, respectively. However, nmSPARSE falls short in optimizing data locality and lacks sparsity-aware memory enhancements, leaving room for further improvements with our approach.

The NM-SpMM is plotted with a black solid line. Besides the $N:M$ sparsity pattern, NM-SpMM leverages hierarchical block algorithms to utilize data locality and applies sparsity-aware optimization. Finally, NM-SpMM outperforms other methods. For instance, at sparsity levels of 50.0%, 62.5%, 75.0%, and 87.5%, our work achieves speedups of 1.8x, 2.4x, 3.5x, and 6.3x over cuBLAS, and speedups of 1.5x, 1.8x, 1.5x, and 1.2x over nmSPARSE, respectively.

On the 3090 and 4090, where there’s a larger gap between SM computing power and memory bandwidth (see Table III), NM-SpMM shows smaller performance gains from $N:M$ sparsity but still surpasses other methods. Overall, NM-SpMM is 2.1x faster than nmSPARSE, with speedup over cuBLAS ranging from 1.4x to 6.3x.

E. Roofline Analysis

We conduct a roofline analysis on NM-SpMM with an input matrix with dimensions $m = n = k = 4096$ on the A100 platform. The experimental results is illustrated in Figure 10. We select four representative sparsity levels. In the figure, the TFLOPS on the vertical axis were collected using NVIDIA’s Nsight Compute(NCU), while the arithmetic intensity on the horizontal axis was calculated using Equation 3. The NCU locks the SM frequency to a specific value during profiling, resulting in a measured peak performance of 14.7 TFLOPS for FP32 CUDA cores. NM-SpMM (indicated by the red markers) achieve 96%, 93%, 95%, and 88% of peak performance at sparsity levels of 50.0%, 62.5%, 75%, and 87.5%, respectively. In contrast, nmSPARSE, represented by the blue markers, only reach 64%, 63%, 49%, and 73%. At sparsity levels of 75.0% and 87.5%, NM-SpMM’s optimization to reduce memory footprint results in a higher arithmetic intensity compared to nmSPARSE. At sparsity levels of 50.0% and

62.5%, the limited capacity of shared memory prevents the use of larger k_s and w_s . Larger k_s and w_s could lead to higher arithmetic intensity, ultimately resulting in NM-SpMM having a higher arithmetic intensity at a sparsity level of 75.0% compared to 62.5%. This experiment highlights the superiority of $N:M$ sparsity in hardware computation and validates the effectiveness of our optimization measures.

V. CONCLUSION

In conclusion, $N:M$ sparsity has proven to be a highly effective strategy to improve DNN inference performance and reduce model size. However, current GPU implementations for $N:M$ sparsity either lack generality or fail to deliver optimal performance. In this work, we propose NM-SpMM, a novel approach that efficiently implements vector-wise $N:M$ sparsity. By incorporating hierarchical blocking mechanism and sparsity-aware optimization, NM-SpMM significantly outperforms existing solutions. Our experiments show that NM-SpMM achieves a speedup of 2.1x compared to nmSPARSE and delivers speedups ranging from 1.4x to 6.3x over cuBLAS. This performance approaches the theoretical maximum speedup enabled by sparsity. This advancement underscores the potential of $N:M$ sparsity to enhance performance in deep learning applications.

VI. ACKNOWLEDGMENT

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